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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/668,236	09/24/2003	Frederic Reblewski	003921.00178	2050
22907	7590	10/14/2005		EXAMINER
BANNER & WITCOFF				TRAN, ANH Q
1001 G STREET N W				
SUITE 1100			ART UNIT	PAPER NUMBER
WASHINGTON, DC 20001				2819

DATE MAILED: 10/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	Application No.	Applicant(s)
	10/668,236	REBLEWSKI ET AL. 
	Examiner Anh Q. Tran	Art Unit 2819

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) Responsive to communication(s) filed on 06 July 2004.
- 2a) This action is FINAL.                            2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) Claim(s) 10-12 and 23 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) Claim(s) \_\_\_\_\_ is/are allowed.
- 6) Claim(s) 10-12 and 23 is/are rejected.
- 7) Claim(s) \_\_\_\_\_ is/are objected to.
- 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on \_\_\_\_\_ is/are: a) accepted or b) objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) All    b) Some \* c) None of:
  1. Certified copies of the priority documents have been received.
  2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413)
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Mail Date. _____
3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date <u>7/6/04</u> .	5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)
	6) <input type="checkbox"/> Other: _____

## DETAILED ACTION

### ***Double Patenting***

1. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

2. Claims 10-12, 13 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims claims 1, 5, 10-12, and 17-18 of U.S. Patent No. 6,947,882. Although the conflicting claims are not identical, they are not patentably distinct from each other because the claimed limitations are found in claims 1, 15, 10-12, and 17-18 of U.S. Patent No. 6,947,882.

### ***Claim Rejections - 35 USC § 102***

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 10-12 are rejected under 35 U.S.C. 102(b) as being anticipated by Trimberger (5,701,44).

Claim 10, Trimberger discloses a multi-clocked routing chip for use in an emulation system, the multi-clocked routing chip comprising:

a reconfigurable static routing circuit (See Col. 1, lines 8-1 1, for the disclosure of programmable or reconfigurable routing matrices); a first set of input/output circuitry coupled to provide inputs to and receive outputs from the reconfigurable static routing circuit (See Col 1, lines 8-1 1, for the disclosure of configurable logic blocks (or input/output circuitry) with programmable routing matrices or circuits),

wherein the first set of input/output circuitry is clocked by a first clock signal (See Col. 24, Section 8.2a Multiple Clocks/Asynchronous Clocking for the disclosure of more than one clock. Also See Figure 27, and the description in Col. 24, lines 55-65 for the signal provided by the user clock, in this Figure the signal provided to the flip flop is slower than the AND gate); and a second set of input/output circuitry coupled to provide inputs to and receive outputs from the reconfigurable static routing circuit (See Col 1, lines 8-1 1, for the disclosure of multiple i.e. two or more configurable logic blocks (or input/output circuitry) with programmable routing matrices or circuits),

wherein the second set of input/output circuitry is clocked by a second clock signal different than the first clock signal (See Col. 24, Section 8.2a Multiple Clocks/Asynchronous Clocking for the disclosure of more than one clock. See Figure 27, and the description in Col. 24, lines 55-65 for the signal provided by the user clock, in this Figure the signal provided to the flip flop is slower than the user clock or a second clock signal. According to this reference Col. 24, lines 42-43, the multiple clock signals may or may not be multiples of the user (first) clock signal).

Claim 11, Trimberger discloses the first and second sets of input/output circuitry each includes a plurality of one-to-n demultiplexers and a plurality of n-to-one multiplexers, where n is an integer greater than 1 (See Figure 52 and description in Col. 35, lines 13 et Seq. for a one-to-n demultiplexer and See Figure 58, item 5601A for input/output circuitry with n-to-one multiplexers).

Claim 12, Trimberger discloses a third set of input/output circuitry coupled to provide inputs to and receive outputs from the reconfigurable static routing circuit, wherein the third set of input/output circuitry is clocked by a third clock signal different than the first and second clock signals (See Figure 228 and text in Col 20, line 58 to Col. 21 line 6, for the third micro cycle or clock signal 2214).

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anh Q. Tran whose telephone number is 571-272-1813. The examiner can normally be reached on M-F (8:00-5:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Pascal can be reached on 571-272-1769. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ANH Q. TRAN  
PRIMARY EXAMINER



10/7/05